Amendments to the Claims:

This listing of claims will replace all prior versions, and lists, of claims in the application:

1. (Currently amended) A computer system comprising:

a central processing unit;

a memory module, said memory module comprising a first memory bank of substantially identical memory chips, a second memory bank of substantially identical memory chips, and a plurality of system bus connectors, said first and second memory banks each comprising a plurality of pin assignments, one pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks, wherein said non-identical pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement; and,

a system bus coupling said central processing unit to said plurality of system bus connectors of said memory module, wherein said central processing unit places information on said system bus mapped to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said information mapped to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

2. (Original) A computer system according to claim 1, wherein said central processing unit further comprises a basic input output system program and a processor, said processor executing said basic input output system program, wherein said processor places said information on said system bus, said information arranged by said basic input output system in said first pattern when accessing said first memory bank, and in said second pattern when accessing said second memory bank.

3. (Original) A computer system according to claim 2, further comprising an operating system loaded into said memory device and executed by said processor, said operating system arranged to communicate information to said basic input output system, wherein said basic input output system arranges said information in a first pattern when said processor accesses said first memory bank, and a second pattern when said processor accesses said second memory bank.

4. (Original) A computer system according to claim 1, wherein said memory module further comprises a plurality of memory modules, and said computer system further comprises a memory controller, said address bus coupling said central processing unit to said memory controller, and said memory controller to each of said plurality of memory modules.

5. (Previously Presented) A computer system according to claim 1, wherein said memory module further comprises:

a substrate;

at least one memory chip mounted on said substrate defining said first memory bank, each said at least one memory chip comprising a plurality of pins, one pin associated with a respective one of said plurality of pin assignments;

at least one memory chip mounted on said substrate defining said second memory bank, each said memory chip comprising a plurality of pins, one pin associated with a respective one of said plurality of pin assignments; and,

a plurality of circuit traces, each circuit trace coupling one pin assignment from each said first and second memory banks to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks and wherein said plurality of system bus connectors comprises a plurality of pads mounted along one edge of said substrate.

6. (Original) A computer system according to claim 5, wherein said substrate further comprises a first major surface and a second major surface, said first memory bank mounted to said first major surface of said substrate, and said second memory bank mounted to said second major surface of said substrate.

7. (Original) A computer system according to claim 6, wherein said first and second memory banks comprise the identical number and configuration of memory chips, and said memory chips mounted on said second major surface of said substrate align in register with said memory chips mounted on said first major surface.

8. (Original) A computer system according to claim 7, wherein said substrate further comprises a plurality of vias, each of said vias adjacent to, and coupling a select one of said plurality of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface.

9. (Previously Presented) A computer system according to claim 8, wherein:

said plurality of system bus connectors further comprise a plurality of address bus connectors;

each said memory chip comprises a plurality of address pins arranged bilaterally symmetrical;

each of said plurality of address pins is associated with a respective one of said plurality of pin assignments; and,

said plurality of vias positioned on said substrate such that each via is adjacent to, and couples a select one of said plurality of address pins comprising a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of address bus connectors.

10. (Original) A computer system according to claim 9, wherein said system bus further comprises an address bus coupled between said central processing unit and said address bus connectors, wherein said central processing unit places an address on said address bus mapped to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said address mapped to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

11. (Original) A computer system according to claim 10, wherein said address comprises a plurality of address bits, said first pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin assignments of said address pins of said first memory bank, and said second pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin assignments of said address pins of said second memory bank.

12. (Previously Presented) A computer system according to claim 8, wherein:

said plurality of system bus connectors further comprise a plurality of command bus connectors;

each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical;

each of said plurality of command pins associated with a respective one of said plurality of pin assignments; and,

said plurality of vias are arranged on said substrate such that each via is adjacent to, and couples a select one of said plurality of command pins comprising a first pin assignment and positioned on said first major surface, to a select one of said plurality of command pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of command bus connectors.

13. (Original) A computer system according to claim 12, wherein said system bus further comprises a command bus coupled between said central processing unit and said command bus connectors, wherein said central processing unit places a command on said command bus mapped to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said command mapped to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

14. (Original) A computer system according to claim 13, wherein said command comprises a plurality of command bits, said first pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins of said first memory bank, and said second pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins defining said second memory bank.

15. (Currently amended) A computer system comprising:

a central processing unit comprising a processor and a basic input output system program;

a memory module, said memory module comprising a first memory bank of substantially identical memory chips, a second memory bank of substantially identical memory chips, and a plurality of system bus connectors;

said first and second memory banks each comprising a plurality of pin assignments, respective pin assignments of said first memory bank correspond to functions that are identical to functions corresponding to respective pin assignments on said second memory bank, each pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of system bus connectors is coupled to non-identical pin assignments of said first and second memory banks, wherein said

non-identical pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement;

a system bus coupling said central processing unit to said plurality of system bus connectors of said memory module, wherein said central processing unit places information on said system bus corresponding to a function associated with at said pin assignments, said information comprising a plurality of bits arranged in a bit pattern, said bit pattern arranged by said basic input output system to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said bit pattern arranged to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

16. (Currently amended) A computer system comprising:

a central processing unit comprising a processor and a basic input output system program;

a memory module, said memory module comprising a first memory bank of substantially identical memory chips, a second memory bank of substantially identical memory chips, and a plurality of system bus connectors, said first and second memory banks each comprising a plurality of system pin assignments, each of said plurality of system bus connectors connecting to an associated one of said plurality of system pin assignments of said first memory bank, and to an associated one of said plurality of system pin assignments of said second memory bank, wherein at least one of said plurality of system bus connectors connects to non identical system pin assignments of said first and second memory banks, wherein said non-identical pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement;

an operating system run by said processor; and,

a system bus coupling said central processing unit to said plurality of system bus connectors of said memory module, wherein said operating system requests information from said processor, and said processor places said information on said system bus mapped by said basic input output system to a first pattern corresponding with said system pin assignments of

said first memory bank when accessing said first memory bank, and mapped to a second pattern corresponding with said address pin assignments of said second memory bank when accessing said second memory bank.

17. (Currently amended) A computer system comprising:

a central processing unit;

a memory module, said memory module comprising:

an address bus connector;

a first memory bank of substantially identical memory chips, said first memory bank comprising a plurality of address pin assignments coupled to said address bus connector in a first pattern; and,

a second memory bank of substantially identical memory chips, said second memory bank comprising a plurality of address pin assignments coupled to said address bus connector in a second pattern, wherein said first and second patterns are not identical such that an address at said address bus connector corresponds to a first address read by said first memory bank, and a second address different from said first address read by said second memory bank, wherein said first address and said second address pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement; and,

an address bus coupling said central processing unit to said address bus connector of said memory module, wherein said central processing unit places an address on said address bus mapped to correspond with said first pattern when accessing said first memory bank, and mapped to correspond with said second pattern when accessing said second memory bank.

18. (Currently amended) A computer system comprising:

a central processing unit;

a system bus coupled to said central processing unit, said system bus comprising a

plurality of system bus lines, each of said plurality of system bus lines corresponding to a unique system bus assignment; and,

a memory device comprising:

a system bus connector coupled to said system bus, said system bus connector comprising a plurality of bus line connectors, each of said plurality of bus line connectors arranged to correspond with a respective one of said system bus lines;

a first memory bank comprising a plurality of substantially identical memory chips and a plurality of pins, each said pin corresponding to a unique pin assignment, each of said address pin assignments connected to an associated one of said plurality of bus line connectors such that said pin assignments of said first memory bank are identical to said system bus assignments; and,

a second memory bank comprising a plurality of substantially identical memory chips and a plurality of pin assignments, each of said pin assignments connected to an associated one of said plurality of bus line connectors such that said pin assignments of said second memory bank are not identical to said system bus assignments, wherein said pin assignments of said first memory bank and said pin assignments of said second memory bank have internal assignments for like functions in a bilaterally symmetrical arrangement, wherein said central processing unit communicates with said memory device by placing information on said system bus, and reading information from said system bus, said information comprising a plurality of bits, each bit associated with one system bus line, and wherein said central processing unit is configured to encode information placed on said system bus to a coded pattern when interfacing with said second memory bank.

19. (Original) A computer system according to claim 18, wherein said coded pattern is defined by rearranging said bits defining said information to correspond to said pin assignments of said second memory bank.

20. (Currently amended) A computer system comprising:

a central processing unit, said central processing unit comprising a processor and a basic input output system program;

a memory module, said memory module comprising a first memory bank of substantially identical memory chips, a second memory bank of substantially identical memory chips, and a plurality of system bus connectors, said first and second memory banks each comprising a plurality of pin assignments, one pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks, wherein said non-identical pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement; and,

a system bus comprising a plurality of physical bus lines, each of said physical bus lines coupling said central processing unit to a respective one of said plurality of system bus connectors of said memory module, said system bus arranged to transfer information between said memory module and said central processing unit, said information comprising a plurality of logical bits, one logical bit per physical bus line, wherein said basic input output system is configured to arrange said information in a first pattern by ordering said plurality of logical bits to bit positions that correspond to said pin assignments of said first memory bank, and said basic input output system is configured to arrange said information in a second pattern by ordering said plurality of logical address bits to bit positions that correspond to said address assignments of said second memory bank.

21. (Original) A computer system according to claim 20, wherein an assignment of at least one logical bit does not correspond with a physical bit assignment of a corresponding physical bus line, but said assignment of said at least one logical bit does correspond with an associated pin assignment to which said at least one logical bit is coupled.

22. (Currently amended) A computer system comprising:

a central processing unit comprising a plurality of system bus connectors, each of said system bus contacts corresponding to a unique bus assignment;

a system bus comprising a plurality of system bus lines;

a remap multiplexer switchable from a first state wherein each of said system bus lines are coupled to a corresponding one of said system bus connectors, to a second state wherein at least two of said bus lines are swapped so as to couple to different ones of said system bus connectors; and

a memory module coupled to said system bus, said memory module comprising a first memory bank of substantially identical memory chips, a second memory bank of substantially identical memory chips, and a plurality of system bus connectors, said first and second memory banks each comprising a plurality of pin assignments, one pin assignment from each said first and second memory banks coupled to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks, wherein said non-identical pin assignments have internal assignments for like functions in a bilaterally symmetrical arrangement, and each of said plurality of system bus connectors coupling to a corresponding one of said system bus lines.

23. (Original) A computer system according to claim 22, wherein said remap multiplexer comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second inputs, an output and a control input, wherein a first one of said system bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said system bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers configured to switch between a first state where said first one of said system bus lines appears at

said output of said first multiplexer and said second one of said system bus lines appears at said output of said second multiplexer, and a second state where said second one of said system bus lines appears at said output of said first multiplexer and said first one of said system bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs.

24. (Previously Presented) A computer system according to claim 23, further comprising:

a memory controller coupled to said system bus, said memory controller connected to said control input of each of said first and second multiplexers, wherein said memory controller is configured to toggle said first and second multiplexers in said first state when said central processing unit communicates with said first memory bank, and said memory controller is configured to switch said first and second multiplexers to said second state when said central processing unit communicates with said second memory bank.

25. (Original) A computer system according to claim 24, wherein said remap multiplexer is coupled to said system bus between said central processing unit and said memory controller.

26. (Original) A computer system according to claim 24, wherein said remap multiplexer is coupled to said system bus between said memory controller and said memory device.

27. (Original) A computer system according to claim 24, wherein said remap multiplexer is integral with said memory controller.

28. (Original) A computer system according to claim 27, wherein said memory controller comprises a buffered system bus driver between said remap multiplexer and said memory device.

29. (Original) A computer system according to claim 28, wherein said memory controller

comprises a buffered system bus register, wherein said remap multiplexer is coupled to said system bus between said buffered system bus register and said memory device.

30. (Previously Presented) A computer system according to claim 24, wherein said memory modu e further comprises:

a substrate;

at least one memory chip mounted on said substrate defining said first memory bank, each said memory chip comprising a plurality of pins, one pin associated with a respective one of said plurality of pin assignments;

at least one memory chip mounted on said substrate defining said second memory bank, each said memory chip comprising a plurality of pins, one pin associated with a respective one of said plurality of pin assignments; and,

a plurality of circuit traces, each circuit trace coupling one pin assignment from each said first a id second memory banks to an associated one of said plurality of system bus connectors, wherein at least one of said plurality of bus connectors is coupled to non-identical pin assignments of said first and second memory banks and wherein said plurality of system bus connectors comprises a plurality of pads mounted along one edge of said substrate.

31. (Original) A computer system according to claim 30, wherein said substrate further comprises a first major surface and a second major surface, said first memory bank mounted to said first major surface of said substrate, and said second memory bank mounted to said second major surface of said substrate.

32. (Original) A computer system according to claim 31, wherein said first and second memory banks comprise the identical number and configuration of memory chips, and said memory chips mounted on said second major surface of said substrate align in register with said memory chips mounted on said first major surface.

33. (Original) A computer system according to claim 32, wherein said substrate further comprises a plurality of vias, each of said vias adjacent to, and coupling a select one of said plural ty of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface.

34. (Previously Presented) A computer system according to claim 33, wherein:

said plurality of system bus connectors further comprise a plurality of address bus connectors;

each said memory chip comprises a plurality of address pins arranged bilaterally symm etrical;

each of said plurality of address pins associated with a respective one of said plurality of pin assignments; and,

said plurality of vias are arranged on said substrate such that each via is adjacent to, and coupling a select one of said plurality of address pins comprising a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of address bus connectors.

35. (Original) A computer system according to claim 34, wherein said system bus further comprises an address bus coupling said central processing unit, said memory controller, said remap multiplexer and said address bus connectors, wherein said central processing unit places an address on said address bus and said remap multiplexer maps said address to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said remap multiplexer maps said address to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

36. (Original) A computer system according to claim 35, wherein said address comprises a plura ity of address bits, said first pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin assignments of said address pins of said first memory bank, and said second pattern comprises arranging said plurality of address bits in a sequence that aligns with the corresponding pin assignments of said address pins defining said secor d memory bank.

37. (Original) A computer system according to claim 35, wherein said remap multiplexer comprises a multiplexing circuit for each pair of bilaterally symmetrical address pins, each of said multiplexing circuits arranged to switchably swap address lines associated with said respective symmetrical address pins.

38. (Original) A computer system according to claim 35, wherein each said multiplexing circuit comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second input, an output and a control input, wherein a first one of said address bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said address bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers switching between a non-switched state where said first one of said address bus lines appears at said output of said first multiplexer and said second one of said address bus lines appears at said output of said second multiplexer, and a switched state where said second one of said address bus lines appears at said output of said first multiplexer and said first one of said address bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs.

39. (Original) A computer system according to claim 37, wherein said memory controller has a

control signal coupled to each said control inputs of said first and second multiplexers of each said multiplexing circuits, said memory controller arranged to switch said control inputs such that all said first and second multiplexers are in said non-switched state or all said first and second multiplexers are in said switched state.

40. (Previously Presented) A computer system according to claim 33, wherein:

said plurality of system bus connectors further comprise a plurality of command bus connectors;

each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical;

each of said plurality of command pins associated with a respective one of said plurality of pin assignments; and,

said plurality of vias arranged on said substrate such that each via is adjacent to, and coup ing a select one of said plurality of command pins comprising a first pin assignment and posit.oned on said first major surface, to a select one of said plurality of command pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of command bus connectors.

41. (Original) A computer system according to claim 40, wherein said system bus further comprises a command bus coupling said central processing unit, said memory controller, said remap multiplexer and said command bus connectors, wherein said central processing unit places a command on said command bus and said remap multiplexer maps said command to a first pattern corresponding with said pin assignments of said first memory bank when accessing said first memory bank, and said remap multiplexer maps said command to a second pattern corresponding with said pin assignments of said second memory bank when accessing said second memory bank.

42. (Original) A computer system according to claim 41, wherein said command comprises a plurality of command bits, said first pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins of said first memory bank, and said second pattern comprises arranging said plurality of command bits in a sequence that aligns with the corresponding pin assignments of said command pins defining said second memory bank.

43. (Original) A computer system according to claim 41, wherein said remap multiplexer comprises a multiplexing circuit for each pair of bilaterally symmetrical command pins, each of said multiplexing circuits arranged to switchably swap command lines associated with said respective symmetrical command pins.

44. (Original) A computer system according to claim 43, wherein each said multiplexing circuit comprises first and second multiplexers, each of said first and second multiplexers comprising a first and second input, an output and a control input, wherein a first one of said command bus lines is coupled to said first input of said first multiplexer and to said second input of said second multiplexer, and a second one of said command bus lines is coupled to said second input of said first multiplexer and said first input of said second multiplexer, said first and second multiplexers switching between a non-switched state where said first one of said command bus lines appears at said output of said first multiplexer and said second one of said command bus lines appears at said output of said second multiplexer, and a switched state where said second one of said command bus lines appears at said output of said first multiplexer and said first one of said command bus lines appears at said output of said second multiplexer based upon a control signal appearing at said control inputs.

45. (Original) A computer system according to claim 44, wherein said memory controller has a control signal coupled to each said control inputs of said first and second multiplexers of each

said multiplexing circuits, said memory controller arranged to switch said control inputs such that all said first and second multiplexers are in said non-switched state or all said first and second multiplexers are in said switched state.

46. (Canceled)

47. (Canceled)

48. (Currently amended) An integrated circuit memory chip comprising:

a circuit package;

a first multiplexer contained within said circuit package of said integrated circuit memory chip, said first multiplexer comprising a first input, a second input, a control signal input, and an output;

a second multiplexer contained within said circuit package of said integrated circuit memory chip, said second multiplexer comprising a first input, a second input, a control signal input, and an output;

a first pin extending from said circuit package and coupled to said first input of said first multiplexer and said second input of said second multiplexer;

a second pin extending from said circuit package and coupled to said second input of said first multiplexer and said first input of said second multiplexer;

a first pin assignment coupled to said output of said first multiplexer;

a second pin assignment coupled to said output of said second multiplexer; and,

a circuit coupled to said first and second pin assignments, wherein said first and second multiplexers are switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output.

49. (Previously Presented) An integrated circuit memory chip according to claim 48, wherein said first and second pins are arranged on said circuit package in a bilaterally symmetrical arrangement.

50. (Previously Presented) An integrated circuit memory chip according to claim 48, further comprising a third pin extending from said circuit package and coupled to said control signal input of said first and second multiplexers.

51. (Previously Presented) An integrated circuit memory chip according to claim 48, wherein said control signal input of said first and second multiplexers are coupled to internal logic, said internal logic arranged to switch said first and second multiplexers between said first and second states.

52. (Previously Presented) An integrated circuit memory chip according to claim 51, wherein said internal logic comprises a mode register.

53. (Currently amended) An integrated circuit memory chip comprising:

a circuit package;

a circuit contained within said circuit package;

a plurality of pins extending from said circuit package; and,

a remap multiplexer contained within said circuit package of said integrated circuit memory chip, said ~~reroute~~ remap multiplexer comprising:

a first multiplexer comprising a first input, a second input, a control signal input, and an output, said first input coupling to a first one of said pins and said second input coupled to a second one of said pins;

a second multiplexer comprising a first input, a second input, a control signal input, and an output, said first input coupled to said second one of said pins and said

second input coupled to said first one of said pins;

a first pin assignment coupling said output of said first multiplexer to said circuit; and,

a second pin assignment coupling said output of said second multiplexer to said circuit, wherein said remap multiplexer is switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output.

54. (Previously Presented) An integrated circuit memory chip according to claim 53, wherein said control signal input of said first and second multiplexers are each coupled to a third one of said plurality of pins on said circuit package.

55. (Previously Presented) An integrated circuit memory chip according to claim 53, wherein said control signal inputs of said first and second multiplexers are coupled to internal logic, said internal logic arranged to switch said remap multiplexer between said first and second states.

56. (Previously Presented) An integrated circuit memory chip according to claim 55, wherein said internal logic comprises a mode register.

57. (Previously Presented) An integrated circuit memory chip comprising:

a circuit package;

a plurality of pins extending from said circuit package;

an memory circuit internal to said circuit package;

a plurality of pin assignments coupled to said memory circuit; and,

a remap multiplexer contained within said circuit package of said integrated circuit memory chip, said remap multiplexer coupling said plurality of pins to said plurality of internal

pin assignments, and comprising a control input, wherein said control signal is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments.

58. (Currently amended) A memory module comprising:

a substrate;

at least one memory chip mounted on said substrate defining a first memory bank, each said at least one memory chip comprising:

a circuit package within said memory chip;

a plurality of pins extending from said circuit package;

an memory circuit internal to said circuit package;

a plurality of pin assignments coupled to said memory circuit; and,

a remap multiplexer contained within said circuit package of said memory chip, said remap multiplexer coupling said plurality of pins to said plurality of internal pin assignments, and comprising a control input, wherein said control signal is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments;

at least one additional memory chip substantially identical to said at least one memory chip mounted on said substrate defining a second memory bank, said additional memory chip comprising:

a circuit package within said at least one additional memory chip;

a plurality of pins extending from said circuit package;

an memory circuit internal to said circuit package;

a plurality of pin assignments coupled to said memory circuit; and,

a remap multiplexer contained within said circuit package of said at least one

additional memory chip, said remap multiplexer coupling said plurality of pins to said plurality of internal pin assignments, and comprising a control input, wherein said control signal input is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments, wherein said pin assignments of said first memory bank and said pin assignments of said second memory bank have internal assignments for like functions;

a plurality of pads mounted along one edge of said substrate; and,

a plurality of circuit traces, each circuit trace coupling one pad to said first and second memory banks.

59. (Original) A memory module according to claim 58, wherein said substrate further comprises a first major surface and a second major surface, said first memory bank mounted to said first major surface of said substrate, and said second memory bank mounted to said second major surface of said substrate.

60. (Original) A memory module according to claim 59, wherein said first and second memory banks comprise the identical number and configuration of memory chips, and said memory chips mounted on said second major surface of said substrate align in register with said memory chips mounted on said first major surface.

61. (Original) A memory module according to claim 60, wherein said substrate further comprises a plurality of vias, each of said vias adjacent to, and coupling a select one of said plurality of pins on said memory chips on said first major surface to a select one of said plurality of pins on said memory chips on said second major surface.

62. (Previously Presented) A memory module according to claim 61, wherein:

each said memory chip comprises a plurality of address pins arranged bilaterally symmetrical;

each of said plurality of address pins is associated with a respective one of a plurality of internal address pin assignments; and,

said plurality of vias positioned on said substrate such that each via is adjacent to, and couples a select one of said plurality of address pins comprising a first pin assignment and positioned on said first major surface, to a select one of said plurality of address pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of circuit traces, and wherein said remap multiplexers in said first bank are switched to said first state, and said remap multiplexers in said second bank are switched to said second state.

63. (Previously Presented) A memory module according to claim 61, wherein:

each said memory chip comprises a plurality of command pins arranged bilaterally symmetrical;

each of said plurality of command pins associated with a respective one of a plurality of internal control pin assignments; and,

said plurality of vias are arranged on said substrate such that each via is adjacent to, and couples a select one of said plurality of command pins comprising a first pin assignment and positioned on said first major surface, to a select one of said plurality of command pins comprising a second pin assignment different from said first pin assignment, and located on said second major surface, to a respective one of said plurality of circuit traces, and wherein said remap multiplexers in said first bank are switched to said first state, and said remap multiplexers in said second bank are switched to said second state.

64. (New) An integrated circuit memory chip comprising:

a circuit package;

a first multiplexer contained within a memory controller of said circuit package said first multiplexer comprising a first input, a second input, a control signal input, and an output;

a second multiplexer contained within a memory controller of said circuit package said second multiplexer comprising a first input, a second input, a control signal input, and an output;

a first pin extending from said circuit package and coupled to said first input of said first multiplexer and said second input of said second multiplexer;

a second pin extending from said circuit package and coupled to said second input of said first multiplexer and said first input of said second multiplexer;

a first pin assignment coupled to said output of said first multiplexer;

a second pin assignment coupled to said output of said second multiplexer; and,

a circuit coupled to said first and second pin assignments, wherein said first and second multiplexers are switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output.

65. (New) An integrated circuit memory chip comprising:

a circuit package;

a circuit contained within said circuit package;

a plurality of pins extending from said circuit package; and,

a remap multiplexer contained within a memory controller of said circuit package, said remap multiplexer comprising:

a first multiplexer comprising a first input, a second input, a control signal input, and an output, said first input coupling to a first one of said pins and said second input coupled to a second one of said pins;

a second multiplexer comprising a first input, a second input, a control signal input, and an output, said first input coupled to said second one of said pins and said second input coupled to said first one of said pins;

a first pin assignment coupling said output of said first multiplexer to said circuit; and,

a second pin assignment coupling said output of said second multiplexer to said circuit, wherein said remap multiplexer is switchable between a first state wherein each said first and second multiplexers connect said first input to said output, and a second state wherein each said first and second multiplexers connect said second input to said output.

66. (New) An integrated circuit memory chip comprising:

a circuit package;

a plurality of pins extending from said circuit package;

an memory circuit internal to said circuit package;

a plurality of pin assignments coupled to said memory circuit; and,

a remap multiplexer contained within said memory circuit of said circuit package, said remap multiplexer coupling said plurality of pins to said plurality of internal pin assignments, and comprising a control input, wherein said control signal is switchable from a first state where said remap multiplexer couples said plurality of pins to said internal pin assignments, to a second state where said remap multiplexer routes at least one of said pins to a different one of said internal pin assignments.